REMARKS

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 1-2, 4-7, and 9 have been amended. New claim 10 has been added. Claims 1-7 and 9-10 are currently pending and under consideration.

Applicants have timely filed a Request for Continued Examination (RCE) along with this Amendment, including the filing fee as set forth in 37 CFR 1.17(e). Accordingly, Applicants respectfully request that the Examiner withdraw the finality of any Office action and enter this Amendment for consideration under 37 CFR 1.114.

Claim Rejections Under 35 USC §§ 112

On page 2 of the Office Action, claims 1-7 and 9 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, the Examiner alleged that the claim language "on an a-by-a basis" is indefinite. This rejection is respectfully traversed.

Applicants respectfully submit that the variable "a" is clearly defined in the claims. For example, claim 1 recites that the variable "a" is a number of M-point radix 2 pipeline FFT circuits each having two parallel inputs/outputs, where "a" is not less than two and is equal to or smaller than M/2. As such, if the value of the variable "a" was 2, for example, then the term "on an a-by-a basis" would be equivalent to the term "on a 2-by-2 basis." Therefore, withdrawal of the rejection is respectfully requested.

Claim Rejections Under 35 USC § 103

On pages 2-3 of the Office Action, claims 1-2 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gray et al. (U.S. Patent No. 4,768,159) in view of Ireland (U.S. Patent No. 5,694,347).

Gray et al. and Ireland, alone or in combination, do not discuss or suggest:

> transform means of a preceding stage including a number a of M-point radix 2 pipeline FFT circuits each having two parallel inputs/outputs, wherein $M(=2^m, m>=2)$ represents a maximum number of points for transform and a, which is not less than two and is equal to or smaller than M/2, represents a divisor of said maximum transform point number M,

as recited in amended claim 1. In other words, the invention of claim 1 provides that the value of variable "a", which represents a number of M-point radix 2 pipeline FFT circuits each having two

parallel inputs/outputs, must be at least two. Since neither Gray et al. nor Ireland discuss or suggest this feature of claim 1, claim 1 patentably distinguishes over the references relied on. Accordingly, withdrawal of this § 103(a) rejection is respectfully requested.

Claims 2-4, 6-7, and 9 depend either directly or indirectly from claim 1 and include all the features of claim 1, plus additional features that are not discussed or suggested by the references relied upon. Therefore, claims 2-4, 6-7, and 9 patentably distinguish over the references relied upon for at least the reasons noted above. Accordingly, withdrawal any § 103(a) rejections is respectfully requested and it is submitted that claims 2-4, 6-7, and 9 are in a condition suitable for allowance.

Gray et al. and Ireland, alone or in combination, do not discuss or suggest:

> said first data supply means is comprised of first and second data permutating modules, said first data permutating module being composed of a first memory circuit for storing data, a read or write address generating circuit which conforms to a predetermined logic of said first memory circuit and a parallel-in serial-out circuit for permutating the data read out from said first memory circuit, while said second data permutating module includes a second memory circuit constituted by two banks so that upon data storing, data are written in said two banks alternately M by M data whereas upon data reading, corresponding data of corresponding data sets each of M point data are simultaneously read out from said two banks, respectively, to constitute two parallel inputs of said pipeline FFT circuit and a read or write address generating circuit which operates in conformance to a predetermined logic of said second memory circuit, and
>
> said second data supply means is comprised of a third memory circuit constituted by two banks so that upon data storing, data are written in said two banks alternately on an M-by-M basis whereas upon data reading, corresponding data of corresponding data sets each of M point data are simultaneously read out from said two banks, respectively, to constitute two parallel inputs of said pipeline FFT circuit and a read or write address generating circuit which operates in conformance to a predetermined logic of said third memory circuit,

as recited in amended claim 5. Gray et al. discloses a method of obtaining sets of m pieces of data from a total of M-by-M pieces of data, in which sets of m pieces of data are obtained in a single stage by means of address translation, in accordance with the order of access, by using an ordinary RAM memory and with the assumption that the total of M-by-M pieces of data is a matrix of size M-by-M. However, in order to achieve high speed performance in the FFT pipeline circuits having two parallel inputs, two pieces of input data are required at the same time and, as such, Gray et al. results in the addresses of these two pieces of data becoming apart from each

other. Thus, in order for a RAM memory to satisfy such a requirement, it is necessary to use a high-function memory, such as a dual port memory, which can access the two addresses at the same time. In contrast, the invention of claim 5 provides for the sorting of data to be carried out in a stepwise manner, such that an ordinary RAM memory can be used.

Since neither Gray et al. nor Ireland discuss or suggest this feature of claim 5, claim 5 patentably distinguishes over the references relied on. Thus, it is submitted that claim 5 is in a condition suitable for allowance.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

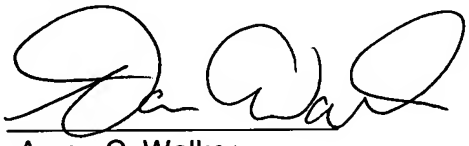
Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 6-17-08

By: 

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